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-	0	2000-0040430	DERWENT	2004/05/26 15:29
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-	0	n99-171734	JPO; DERWENT	2004/05/26 15:35
-	0	"n99-171734"	JPO; DERWENT	2004/05/26 15:35
-	1	"external data storage apparatus"	JPO; DERWENT	2004/05/26 15:45
-	2	("6330634").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/26 15:49
-	2	("6308325").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/26 15:50
-	1	2002/0023177	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/26 15:51
-	0	(2002/0023177).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/26 15:51
-	37	dobbek.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/26 15:51
-	1318	((717/168,170) or (713/100)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 10:43
-	37	ROM near40 flash near40 nonvolatile same version	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 10:24
-	71	firmware same flash near40 voltage	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 10:44
-	1	(((717/168,170) or (713/100)).CCLS.) and (firmware same flash near40 voltage)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 10:24

-	1	(((717/168-173) or (713/100)).CCLS.) and (firmware same flash near40 voltage)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 10:44
-	153	firmware same flash same version	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 10:44
-	18	(((717/168-173) or (713/100)).CCLS.) and (firmware same flash same version)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 13:10
-	6	("5568641" | "5732268" | "5793943" | "6079016" | "6308265" | "6401208").PN.	USPAT	2004/05/27 11:23
-	1036	flash with version	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 13:10
-	1643	((717/168-173) or (713/100)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 13:10
-	51	(flash with version) and (((717/168-173) or (713/100)).CCLS.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/05/27 13:10
-	14	(US-6467087-$ or US-5701492-$ or US-6584559-$ or US-6615404-$ or US-6640334-$ or US-5960445-$ or US-5987605-$ or US-6009520-$ or US-6041319-$ or US-6070012-$ or US-6243809-$ or US-6496978-$ or US-6564318-$).did. or (US-20020085229-$).did.	USPAT; US-PGPUB	2004/05/27 14:15
-	1	WO98/24021	USPAT; US-PGPUB	2004/05/27 14:16

Terms used **ROM flash memory version** Found **113** of **807,214**

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1 Caches and Memory Systems: Patchable instruction ROM architecture
Timothy Sherwood, Brad Calder
November 2001 **Proceedings of the international conference on Compilers, architecture, and synthesis for embedded systems**
Full text available: pdf(299.03 KB) Additional Information: full citation, abstract, references, index terms

Increased systems level integration has meant the movement of many traditionally off chip components onto a single chip including a processor, instruction storage, data path, and local memory. The design of these systems is driven by two conflicting goals, the need for reduced area and the need for rapid development times. The two current design options for instruction storage, ROM and Flash, are each highly optimized to one of these two goals but provide little compromise between them. ROM is u ...

2 System on chip design: Automatic generation of embedded memory wrapper for multiprocessor SoC
Ferid Gharsalli, Samy Meftali, Frédéric Rousseau, Ahmed A. Jerraya
June 2002 **Proceedings of the 39th conference on Design automation**
Full text available: pdf(246.75 KB) Additional Information: full citation, abstract, references, citings, index terms

Embedded memory plays a critical role to improve performances of systems-on-chip (SoC). In this paper, we present a new methodology for embedded memory design in the case of application specific multiprocessor system-on-chip. This approach facilitates the integration of standard memory components. The concept of memory wrapper allows automatic adaptation of physical memory interfaces to a communication network that may have a different number of access ports. We give also a generic architecture ...

Keywords: dystem-on-chip, embedded memory, memory access, memory wrapper generation

3 Pen computing: a technology overview and a vision
André Meyer
July 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 3
Full text available: pdf(5.14 MB) Additional Information: full citation, abstract, citings, index terms

This work gives an overview of a new technology that is attracting growing interest in public as well as in the computer industry itself. The visible difference from other technologies is in the use of a pen or pencil as the primary means of interaction between a user and a machine, picking up the familiar pen and paper interface metaphor. From this follows a set of consequences that will be analyzed and put into context with other emerging technologies and visions.Starting with a short historic ...

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1 **Embedded HIMOS(R) flash memory in 0.35 µm and 0.25 µm CMOS technologies**
Wellekens, D.; Van Houdt, J.; Haspeslagh, L.; Tsouhlarakis, J.; Hendrickx, P.; Deferm, L.; Maes, H.E.;
Electron Devices, IEEE Transactions on , Volume: 47 , Issue: 11 , Nov. 2000
Pages:2153 - 2160

[Abstract] [PDF Full-Text (164 KB)] IEEE JNL

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2 **Implementation of a charge-based neural Euclidean classifier for a 3-bit flash analog-to-digital converter**
Onat, B.M.; McNeill, J.A.; Cilingiroglu, U.;
Instrumentation and Measurement, IEEE Transactions on , Volume: 46 , Issue: 3 , June 1997
Pages:672 - 677

[Abstract] [PDF Full-Text (160 KB)] IEEE JNL

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3 **Searching in parallel for similar strings [biological sequences]**
Rigoutsos, I.; Califano, A.;
Computational Science and Engineering, IEEE [see also Computing in Science & Engineering] , Volume: 1 , Issue: 2 , Summer 1994
Pages:60 - 75

[Abstract] [PDF Full-Text (2196 KB)] IEEE JNL

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4 **A novel sense amplifier for flexible voltage operation NAND flash memories**
Nakamura, H.; Miyamoto, J.; Imamiya, K.; Iwata, Y.;
VLSI Circuits, 1995. Digest of Technical Papers., 1995 Symposium on , 8-10 June 1995
Pages:71 - 72

[Abstract] [PDF Full-Text (192 KB)] IEEE CNF